TECHNISCHE HOCHSCHULE LÜBECK

Module: Applied FPGA and VLSI Design

Level	Master	**Short Name**	AFPGA
Responsible Lecturers	Peter Bartmann, M.Sc.		
Department, Facility	Electrical Engineering and Computer Science		
Course of Studies	Applied Information Technology, Master		
Compulsory/elective	Compulsory elective	**ECTS Credit Points**	5
Semester of Studies	2	**Semester Hours per Week**	4
Length (semesters)	1	**Workload (hours)**	150
Frequency	WiSe	**Presence Hours**	60
Teaching Language	English	**Self-Study Hours**	90

The following section is filled only if there is **exactly one** module-concluding exam.

Exam Type	Portfolio Exam	**Exam Language**	German/English
Exam Length (minutes)		**Exam Grading System**	One-third Grades

Learning Outcomes	After successful completion of the course, students are able to: • Describe and explain conventional and non-conventional number systems • Calculate in non-conventional number systems (add/sub, mult, div) incl. rounding and overflow handling • Implement advanced/optimized adder and multiplication structures in VLSI design • Implement and test digital signal processing pipelines (like polyphase filter) • Compose and analyze timing constraints • Analyze existing arithmetic / logic units, differentiate against other solutions and optimize them according to a given measurement function
Participation Prerequisites	Following knowledge is helpful, but not required to participate. • Experience in hardware description language VHDL or Verilog • Good understanding of linear algebra and number representations • Confidence use/handling of Boolean logic • Basic knowledge in discrete signals and systems

The previous section is filled only if there is **exactly one** module-concluding exam.

Consideration of Gender and Diversity Issues	✔ Use of gender-neutral language (THL standard) ✔ Target group specific adjustment of didactic methods ✘ Making subject diversity visible (female researchers, cultures etc.)
Applicability	

Remarks	

TECHNISCHE HOCHSCHULE LÜBECK

Module Course: Applied FPGA and VLSI Design (Lecture)

(of Module: Applied FPGA and VLSI Design)

Course Type	Lecture	**Form of Learning**	Presence
Mandatory Attendance	no	**ECTS Credit Points**	3
Participation Limit		**Semester Hours per Week**	3
Group Size		**Workload (hours)**	90
Teaching Language	English	**Presence Hours**	45
Study Achievements ("Studienleistung", SL)		**Self-Study Hours**	45
SL Length (minutes)		**SL Grading System**	

The following section is filled only if there is a course-specific exam.

Exam Type		**Exam Language**	
Exam Length (minutes)		**Exam Grading System**	
Learning Outcomes			
Participation Prerequisites			

The previous section is filled only if there is a course-specific exam.

Contents

- Number representation / number systems
  - recap on conventional systems
  - non-conventional/redundant number systems
  - rounding and overflow in non-conventional systems
- Addition
  - Carry based adder
  - carry-free redundant adder
  - multi-operand and sequential adder
- Multiplication/Division
  - Advanced structures like Braun-Array-Multiplier
  - Pezarris-Array-Multiplier and Booth-Wallace-Multiplier
  - division by multiplication
- Optimization for FPGAs
  - Timing description
  - FPGA-optimized VHDL-coding
- Applications
  - Transformation of algorithms
  - Retiming
  - Multi-rate and polyphase digital filters

Literature

- Amos R. Omondi, Computer Arithmetic Systems Algorithms, Architecture and Implemetations, Prentice-Hall, 1994, ISBN:0-13-334301-4

	• Steve Kilts, Advanced FPGA Design, Architecture, Implementation, and Optimization, Wiley-Interscience, 2007, ISBN: 978-0-470-05437-6 • Israel Koren, Computer Arithmetic Algorithms, http://www.ecs.umass.edu/ece/koren/arith/ • Peter Pirsch, Architekturen der digitalen Signalverarbeitung, B.G. Teubner, Stuttgart, 1996 • Jean-Michel Muller, Elementary Functions, Algorithms and Implementation, Birkhäuser Boston, 2006, http://perso.ens-lyon.fr/jean-michel.muller/SecondEdition.html • Reto Zimmermann, Computer Arithmetic: Principles, Architectures, and VLSI Design, Lecture notes, Integrated Systems Laboratory, ETH Zürich, 1997, http://www.iis.ee.ethz.ch/~zimmi
Remarks	

Module Course: Applied FPGA and VLSI Design (Practical Training)

(of Module: Applied FPGA and VLSI Design)

Course Type	Practical Training	**Form of Learning**	Presence
Mandatory Attendance	yes	**ECTS Credit Points**	2
Participation Limit		**Semester Hours per Week**	1
Group Size		**Workload (hours)**	60
Teaching Language	English	**Presence Hours**	15
Study Achievements ("Studienleistung", SL)		**Self-Study Hours**	45
SL Length (minutes)		**SL Grading System**	
The following section is filled only if there is a course-specific exam.			
Exam Type		**Exam Language**	
Exam Length (minutes)		**Exam Grading System**	
Learning Outcomes			
Participation Prerequisites			
The previous section is filled only if there is a course-specific exam.			
Contents	• Implementation of a multiplication-addition structure (e.g. FIR filter, color space transformation) in VHDL • Testing and evaluation of own implementation • Optimizing VHDL code for a given FPGA • Optimization according to an objective function (combination of error, max. speed, min. size, ...)		
Literature	• Same as lecture • Documentation of used development kits		
Remarks			