

## Module: Applied FPGA and VLSI Design

| Level                 | Master                                      | Short Name              | AFPGA |
|-----------------------|---|-------------------------|-------|
| Responsible Lecturers | Peter Bartmann, M.Sc.                       |                         |       |
| Department, Facility  | Electrical Engineering and Computer Science |                         |       |
| Course of Studies     | Applied Information Technology, Master      |                         |       |
| Compulsory/elective   | Compulsory elective                         | ECTS Credit Points      | 5     |
| Semester of Studies   | 2   | Semester Hours per Week | 4     |
| Length (semesters)    | 1   | Workload (hours)        | 150   |
| Frequency             | WiSe  | Presence Hours          | 60    |
| Teaching Language     | English                                     | Self-Study Hours        | 90    |

## The following section is filled only if there is **exactly one** module-concluding exam.

| Exam Type                                       | Project Work   | Exam Language  | German/English   |
|---|--|--|------------------|
| Exam Length (minutes)                           |  | Exam Grading System  | One-third Grades |
| Learning Outcomes                               | <ul> <li>After successful completion of the course, students are able to:</li> <li>Describe and explain conventional and non-conventional number systems</li> <li>Calculate in non-conventional number systems (add/sub, mult, div) incl. rounding and overflow handling</li> <li>Implement advanced/optimized adder and multiplication structures in VLSI design</li> <li>Implement and test digital signal processing pipelines (like polyphase filter)</li> <li>Compose and analyze timing constraints</li> <li>Analyze existing arithmetic / logic units, differentiate against other solutions and optimize them according to a given measurement function</li> </ul> |  |                  |
| Participation Prerequisites                     | <ul> <li>Following knowledge</li> <li>Experience in</li> <li>Good understarepresentation</li> <li>Confidence us</li> <li>Basic knowled</li> </ul>  | ing knowledge is helpful, but not required to participate.<br>Experience in hardware description language VHDL or Verilog<br>Good understanding of linear algebra and number<br>representations<br>Confidence use/handling of Boolean logic<br>Basic knowledge in discrete signals and systems |                  |
| The previous section is filled onl              | y if there is <b>exactly on</b>  | e module-concluding exam.  |                  |
| Consideration of Gender<br>and Diversity Issues | <ul> <li>Use of gender-ne</li> <li>Target group spe</li> <li>Making subject di</li> </ul>  | neutral language (THL standard)<br>pecific adjustment of didactic methods<br>diversity visible (female researchers, cultures etc.)   |                  |
| Applicability                                   |  |  |                  |

| Remarks |  |
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## Module Course: Applied FPGA and VLSI Design (Lecture)

(of Module: Applied FPGA and VLSI Design)

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|---|--|-------------------------|----------|
| Course rype                                   |  |                         |          |
| Mandatory Attendance                          | no   | ECTS Credit Points      | 3        |
| Participation Limit                           |  | Semester Hours per Week | 3        |
| Group Size                                    |  | Workload (hours)        | 90       |
| Teaching Language                             | English  | Presence Hours          | 45       |
| Study Achievements<br>("Studienleistung", SL) |  | Self-Study Hours        | 45       |
| SL Length (minutes)                           |  | SL Grading System       |          |
| The following section is filled on            | ly if there is a course-s  | pecific exam.           |          |
| Exam Type                                     |  | Exam Language           |          |
| Exam Length (minutes)                         |  | Exam Grading System     |          |
| Learning Outcomes                             |  | ·                       | <u>.</u> |
| Participation Prerequisites                   |  |                         |          |
| The previous section is filled only           | y if there is a course-s   | pecific exam.           |          |
| Contents                                      | <ul> <li>Number representation / number systems <ul> <li>recap on conventional systems</li> <li>non-conventional/redundant number systems</li> <li>rounding and overflow in non-conventional systems</li> </ul> </li> <li>Addition <ul> <li>Carry based adder</li> <li>carry-free redundant adder</li> <li>multi-operand and sequential adder</li> </ul> </li> <li>Multiplication/Division <ul> <li>Advanced structures like Braun-Array-Multiplier</li> <li>Pezarris-Array-Multiplier and Booth-Wallace-Multiplier</li> <li>division by multiplication</li> </ul> </li> <li>Optimization for FPGAs <ul> <li>Timing description</li> <li>FPGA-optimized VHDL-coding</li> </ul> </li> <li>Applications <ul> <li>Transformation of algorithms</li> <li>Retiming</li> <li>Multi-rate and polyphase digital filters</li> </ul> </li> </ul> |                         |          |
| Literature                                    | <ul> <li>Amos R. Omondi, Computer Arithmetic Systems Algorithms,<br/>Architecture and Implemetations, Prentice-Hall, 1994,<br/>ISBN:0-13-334301-4</li> </ul>   |                         |          |

|         | <ul> <li>Steve Kilts, Advanced FPGA Design, Architecture,<br/>Implementation, and Optimization, Wiley-Interscience, 2007,<br/>ISBN: 978-0-470-05437-6</li> <li>Israel Koren, Computer Arithmetic Algorithms, http://<br/>www.ecs.umass.edu/ece/koren/arith/</li> <li>Peter Pirsch, Architekturen der digitalen Signalverarbeitung, B.G.<br/>Teubner, Stuttgart, 1996</li> <li>Jean-Michel Muller, Elementary Functions, Algorithms and<br/>Implementation, Birkhäuser Boston, 2006, http://perso.ens-lyon.fr/<br/>jean-michel.muller/SecondEdition.html</li> <li>Reto Zimmermann, Computer Arithmetic: Principles,<br/>Architectures, and VLSI Design, Lecture notes, Integrated<br/>Systems Laboratory, ETH Zürich, 1997, http://www.iis.ee.ethz.ch/<br/>~zimmi</li> </ul> |
|---------|---|
| Remarks |   |



## Module Course: Applied FPGA and VLSI Design (Practical Training)

(of Module: Applied FPGA and VLSI Design)

| Course TypePractical TrainingForm of LearningPresenceMandatory AttendanceyesECTS Credit Points2Participation LimitSemester Hours per Week1Group SizeEnglishWorkload (hours)60Teaching LanguageEnglishPresence Hours15Study Achievements<br>("Studienleistung", SL)Practical Training<br>("Studienleistung", SL)Self-Study Hours45SL Length (minutes)Practical Training<br>("Studienleistung", SL)PassPassThe following section is filled or<br>Learning OutcomesExam Language<br>(Exam Length (minutes))PassParticipation PrerequisitesImplementation of a multiplication-addition structure (e.g. FIR<br>filter, color space transformation) in VHDL<br>· Testing and evaluation of own implementation -<br>· Optimizing VHDL code for a given FPGA<br>· Optimization according to an objective function of<br>· Optimization according to a                |   |  |                         |          |
|--|---|--|-------------------------|----------|
| Mandatory AttendanceyesECTS Credit Points2Participation LimitSemester Hours per Week1Group SizeWorkload (hours)60Teaching LanguageEnglishPresence Hours15Study Achievements<br>("Studienleistung", SL)Practical TrainingSelf-Study Hours45SL Length (minutes)Practical TrainingSelf-Study Hours45SL Length (minutes)SL Grading SystemPassThe following section is filled only if there is a course-specific exam.PassExam TypeExam Language1Exam TypeExam Grading System1Learning OutcomesExam Grading System1Participation PrerequisitesImplementation of a multiplication-addition structure (e.g. FIR<br>filter, color space transformation) in VHDL<br>· Testing and evaluation of own implementation<br>· Optimizing VHDL code for a given FPGA<br>· Optimization according to an objective function (combination of<br>error, max. speed, min. size,)• Same as lecture<br>· Documentation of used development kitsRemarksSame as lecture<br>· Documentation of used development kits   | Course Type                                   | Practical Training   | Form of Learning        | Presence |
| Participation LimitSemester Hours per Week1Group SizeGoudWorkload (hours)60Teaching LanguageEnglishPresence Hours15Study Achievements<br>("Studienleistung", SL)Practical TrainingSelf-Study Hours45SL Length (minutes)Practical TrainingSelf-Study HoursPassThe following section is filled onlyIthere is a course-specific exam.PassExam TypeExam Grading SystemPassExam Length (minutes)Exam Grading SystemImplementationParticipation PrerequisitesImplementation of a multiplication-addition structure (e.g. FIR<br>filter, color space transformation) in VHDL<br>· Testing and evaluation of own implementation<br>· Optimizing VHDL code for a given FPGA<br>· Optimizing VHDL code for a give | Mandatory Attendance                          | yes  | ECTS Credit Points      | 2        |
| Group SizeWorkload (hours)60Teaching LanguageEnglishPresence Hours15Study Achievements<br>("Studienleistung", SL)Practical TrainingSelf-Study Hours45SL Length (minutes)Practical TrainingSelf-Study Hours45SL Length (minutes)SL Grading SystemPassThe following section is filled only if there is a course-specific exam.Exam Language15Exam TypeExam Grading SystemImplementation15Learning OutcomesExam Grading SystemImplementation structure (e.g. FIR<br>filter, color space transformation) in VHDL<br>. Testing and evaluation of own implementation<br>. Optimizing VHDL code for a given FPGA<br>. Optimization according to an objective function (combination of<br>error, max. sped, min. size,)Same as lecture<br>. Documentation of used development kitsRemarksExam RemarksSame as lecture<br>. Documentation of used development kits   | Participation Limit                           |  | Semester Hours per Week | 1        |
| Teaching LanguageEnglishPresence Hours15Study Achievements<br>("Studienleistung", SL)Practical TrainingSelf-Study Hours45SL Length (minutes)SL Grading SystemPassThe following section is filled only<br>Exam TypeExam LanguagePassExam TypeExam Grading SystemLearning OutcomesExam Grading SystemParticipation PrerequisitesThe previous section is filled only<br>if there is a course-specific exam.Participation Structure for there is a course-specific exam.The previous section is filled only<br>if there is a course-specific exam.ContentsImplementation of a multiplication-addition structure (e.g. FIR<br>filter, color space transformation) in VHDL<br>. Testing and evaluation of own implementation<br>. Optimizing VHDL code for a given FPGA<br>. Optimization according to an objective function (combination of<br>error, max. sped, min. size,)Literature. Same as lecture<br>. Documentation of used development kitsRemarks  | Group Size                                    |  | Workload (hours)        | 60       |
| Study Achievements<br>("Studienleistung", SL)Practical TrainingSelf-Study Hours45SL Length (minutes)SL Grading SystemPassThe following section is filled only if there is a course-specific exam.PassExam TypeExam LanguageExam Length (minutes)Exam Grading SystemLearning OutcomesExam Grading SystemParticipation PrerequisitesThe previous section is filled only if there is a course-specific exam.ContentsImplementation of a multiplication-addition structure (e.g. FIR<br>filter, color space transformation) in VHDL<br>• Testing and evaluation of own implementation<br>• Optimizing VHDL code for a given FPGA<br>• Optimization according to an objective function (combination of<br>error, max. speed, min. size,)LiteratureSame as lecture<br>• Documentation of used development kitsRemarks  | Teaching Language                             | English  | Presence Hours          | 15       |
| SL Length (minutes)SL Grading SystemPassThe following section is filled only if there is a course-specific exam.Exam LanguageExam TypeExam Grading SystemImageExam Length (minutes)Exam Grading SystemImageLearning OutcomesExam Grading SystemImageParticipation PrerequisitesImageImageThe previous section is filled only if there is a course-specific exam.ImageImageContentsImplementation of a multiplication-addition structure (e.g. FIR filter, color space transformation) in VHDL<br>• Testing and evaluation of own implementation<br>• Optimizing VHDL code for a given FPGA<br>• Optimization according to an objective function (combination of error, max. speed, min. size,)• Same as lecture<br>• Documentation of used development kitsRemarksImageImageImage  | Study Achievements<br>("Studienleistung", SL) | Practical Training   | Self-Study Hours        | 45       |
| The following section is filled only if there is a course-specific exam.Exam TypeExam LanguageExam Length (minutes)Exam Grading SystemLearning OutcomesExam Grading SystemParticipation PrerequisitesImplementationThe previous section is filled only if there is a course-specific exam.Implementation addition structure (e.g. FIR filter, color space transformation) in VHDL<br>• Testing and evaluation of own implementation<br>• Optimizing VHDL code for a given FPGA<br>• Optimization according to an objective function (combination of error, max. speed, min. size,)LiteratureSame as lecture<br>  | SL Length (minutes)                           |  | SL Grading System       | Pass     |
| Exam TypeExam LanguageExam Length (minutes)Exam Grading SystemLearning OutcomesExam Grading SystemParticipation PrerequisitesFreequisitesThe previous section is filled on it for a multiplication-addition structure (e.g. FIR filter, color space transformation) in VHDL<br>• Testing and evaluation of own implementation<br>• Optimizing VHDL code for a given FPGA<br>• Optimization according to an objective function (combination of error, max. speed, min. size,)LiteratureSame as lect<br>• Documentation is on used development kitsRemarks  | The following section is filled on            | ly if there is a course-s  | pecific exam.           |          |
| Exam Length (minutes)Exam Grading SystemLearning Outcomes  | Exam Type                                     |  | Exam Language           |          |
| Learning OutcomesParticipation PrerequisitesThe previous section is filled on V if there is a course-specific exam.ContentsImplementation of a multiplication-addition structure (e.g. FIR<br>filter, color space transformation) in VHDL<br>• Testing and evaluation of own implementation<br>• Optimizing VHDL code for a given FPGA<br>• Optimization according to an objective function (combination of<br>error, max. speed, min. size,)LiteratureSame as lecture<br>• Documentation of used development kitsRemarks  | Exam Length (minutes)                         |  | Exam Grading System     |          |
| Participation PrerequisitesThe previous section is filled only if there is a course-specific exam.ContentsImplementation of a multiplication-addition structure (e.g. FIR<br>filter, color space transformation) in VHDL<br>• Testing and evaluation of own implementation<br>• Optimizing VHDL code for a given FPGA<br>• Optimization according to an objective function (combination of<br>error, max. speed, min. size,)Literature• Same as lecture<br>• Documentation of used development kitsRemarks   | Learning Outcomes                             |  |                         |          |
| The previous section is filled only if there is a course-specific exam.         Contents       Implementation of a multiplication-addition structure (e.g. FIR filter, color space transformation) in VHDL         Testing and evaluation of own implementation       Optimizing VHDL code for a given FPGA         Optimization according to an objective function (combination of error, max. speed, min. size,)       Same as lecture         Documentation of used development kits       Documentation of used development kits   | Participation Prerequisites                   |  |                         |          |
| Contents• Implementation of a multiplication-addition structure (e.g. FIR<br>filter, color space transformation) in VHDL<br>• Testing and evaluation of own implementation<br>• Optimizing VHDL code for a given FPGA<br>• Optimization according to an objective function (combination of<br>error, max. speed, min. size,)Literature• Same as lecture<br>• Documentation of used development kitsRemarks   | The previous section is filled onl            | y if there is a course-s   | pecific exam.           |          |
| Literature       • Same as lecture         • Documentation of used development kits         Remarks  | Contents                                      | <ul> <li>Implementation of a multiplication-addition structure (e.g. FIR filter, color space transformation) in VHDL</li> <li>Testing and evaluation of own implementation</li> <li>Optimizing VHDL code for a given FPGA</li> <li>Optimization according to an objective function (combination of error, max. speed, min. size,)</li> </ul> |                         |          |
| Remarks  | Literature                                    | <ul><li>Same as lecture</li><li>Documentation of used development kits</li></ul>   |                         |          |
|  | Remarks                                       |  |                         |          |